DETAILED ACTION

Election/Restrictions

1. Applicant's reply filed on August 25, 2009 is acknowledged that claims 25-31 has been withdrawn. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

2. This application is in condition for allowance except for the presence of claims 25-31 directed to an invention non-elected without traverse. Accordingly, claims 25-31 have been cancelled.

EXAMINER'S AMENDMENT

3. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows: Claims 25-31 are cancelled.

Allowable Subject Matter

4. Claims 1-24 are allowed.

5. The following is an examiner's statement of reasons for allowance: The claims recite a device for joining substrates which is used for manufacturing a chip size package formed in a way that a semiconductor substrate with plural elements formed thereon and a sealing substrate for individually sealing said elements are joined

together and diced into a plurality of said chip size packages having said individual sealed element, comprising:

a substrate supplying section for supplying said semiconductor substrate and said sealing substrate; a transcribing sheet supplying section for supplying an elastic transcribing sheet on which adhesive is coated;

a transcribing sheet pressurization section for pressurizing together a joint surface of said transcribing sheet coated with said adhesive and a joint surface of said sealing substrate;

a transcribing sheet peeling section for peeling said transcribing sheet from said sealing substrate so as to form a layer of said adhesive on said sealing substrate;

a parallelism adjusting section for adjusting parallelism of said joint surface of said semiconductor substrate and said joint surface of said sealing substrate on which said adhesive layer is formed;

a substrate joining section for adjusting positions of said semiconductor substrate and said sealing substrate, and then joining said semiconductor substrate and said sealing substrate which are adjusted their positions;

and a substrate conveying mechanism for conveying said semiconductor substrate, said sealing substrate and said transcribing sheet among said respective sections. Foster discloses a method of forming chip scale optical image sensing integrated circuit. The method includes providing an adhesive matrix, a cover glass, a wafer, adhering the cover glass the wafer using the adhesive matrix, wherein the adhesive matrix includes opening coinciding with the location on the wafer that contain

micro lenses. (Col 2, lines 2-9) Herndon et al discloses a method of forming an optical device. The method includes providing a pre-applied adhesive or adhesive matrix forming between two release liners, removing the first release liner, applying the exposed adhesive to the optically transmissive substrate using a rubber coated roller (Col 3, lines 3-13), dicing or shaping the substrate with the pre-applied adhesive necessary for the optical product prior to removing the second release liner (Col 3, lines 14-17). Furthermore, Lee discloses the adhesive layer or matrix can be applied to the cover and then align with carrier and side wall or spacer (Col 4, lines 38-59). Foster as modified by the combination of Herndon et al and Lee is silent as to the apparatus includes a substrate supplying section, a parallelism adjusting section, substrate joining section, and a substrate conveying mechanism. Kato et al discloses an apparatus for aligning a wafer and a mask or disc substrate. The apparatus includes a wafer carrier movable in parallel direction in the x, y, and θ and aligning the wafer to the mask according the alignment marks on both the mask and wafer (Col 2, lines 27-42) by moving the alignment mark in the x-axis, y-axis, and degree of rotation. Kato et al does not discloses a parallelism adjusting section for adjusting parallelism of said joint surface of said semiconductor substrate and said joint surface of said sealing substrate on which said adhesive layer is formed. A search of prior art of record did not disclose reference or references in combination with the recited feature.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SING P. CHAN whose telephone number is (571)272-1225. The examiner can normally be reached on Monday-Thursday 7:30AM-11:00AM and 12:00PM-4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Philip C. Tucker can be reached on 571-272-1095. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sing P Chan/
Acting Examiner of Art Unit 1791

/Philip C Tucker/
Supervisory Patent Examiner, Art Unit 1791